(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 505 623 A1

(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 158(3) EPC

(43) Date of publication:
**09.02.2005 Bulletin 2005/06**

(21) Application number: **04712215.5**

(22) Date of filing: **18.02.2004**

(51) Int Cl.[7]: **H01J 11/02**

(86) International application number:
**PCT/JP2004/001811**

(87) International publication number:
**WO 2004/075238 (02.09.2004 Gazette 2004/36)**

(84) Designated Contracting States:
**AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR**
Designated Extension States:
**AL LT LV MK**

(30) Priority: **20.02.2003 JP 2003042868**
**13.11.2003 JP 2003383551**

(71) Applicant: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
**Kadoma-shi, Osaka 571-8501 (JP)**

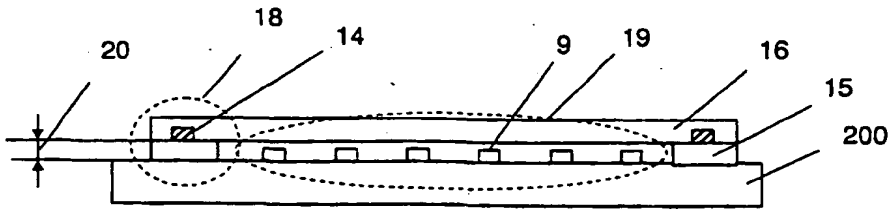
(72) Inventors:
- **TACHIBANA, Hiroyuki**
  **Osaka 560-0021 (JP)**
- **KOSUGI, Naoki**
  **Kyoto-shi, Kyoto 606-8331 (JP)**
- **OKAWA, Masafumi**
  **Osaka 565-0817 (JP)**
- **MURAI, Ryuichi**
  **Toyonaka-shi, Osaka 560-0085 (JP)**

(74) Representative: **Balsters, Robert et al**
**Novagraaf SA**
**25, Avenue du Pailly**
**1220 Les Avanchets - Geneva (CH)**

(54) **PLASMA DISPLAY PANEL**

(57) A highly reliable plasma display panel with less difference in wiring resistance, which can be driven at high speed even though the front or rear board has multilayer electrode wiring. Data electrode (9) is covered with dielectric layer (15), and priming electrode (14) is provided on dielectric layer (15). External wiring lead-out (19) of data electrode (9) is provided on rear substrate (200), and external wiring lead-out (18) of priming electrode (14) is provided on dielectric layer (15). Wiring lead-out (19) and wiring lead-out (18) have step (20) equivalent to the thickness of dielectric layer (15).

FIG.4




EP 1 505 623 A1

Printed by Jouve, 75001 PARIS (FR)

## Description

### TECHNICAL FIELD

**[0001]** The present invention relates to plasma display panels, and more particularly to plasma display panels achieving highly reliable connections in multilayer electrode wiring.

### BACKGROUND ART

**[0002]** Plasma display devices employing plasma display panels (PDPs) are drawing increasing attention as display devices for high-definition television images on large screens.

**[0003]** A PDP is basically composed of front and rear boards. The front board includes a glass substrate, display electrodes including transparent electrodes and bus electrodes aligned in stripes on one main face of the glass substrate, a dielectric layer covering the display electrodes that functions as a capacitor, and a dielectric protective film formed on the dielectric layer. The rear board includes a glass substrate, address electrodes aligned in stripes on one main face, a dielectric layer covering the address electrodes, barrier ribs formed on the dielectric layer, and a phosphor layer which emits red, green, and blue lights formed between barrier ribs.

**[0004]** The electrodes on the front and rear boards face each other, and their peripheries are hermetically sealed. Discharge gas such as neon (Ne) - xenon (Xe) is injected into the discharge space created by the barrier ribs at pressures of 400 - 600 torr. The discharge gas is discharged by selectively applying video signal voltages to the display electrodes. Ultraviolet rays emitted by the discharge gas excite the different color phosphor layers. Red, green, and blue light is thus emitted to display color images.

**[0005]** A wiring lead-out of display electrodes on the front board and address electrodes on the rear board are provided on respective boards in the same plane, and a flexible printed circuit board (FPC) is press-bonded on the lead-out via an anisotropic conductive member to connect to external wiring. One example of a PDP in which these electrodes have a multilayer structure on each board by interposing an insulating layer with a predetermined thickness is disclosed in Japanese Laid-open Patent No. 2 001-210243. In this example, the electrode wiring layer on the front board has scanning electrodes and susutain electrodes as the first electrode layer, and trigger electrodes separated by the dielectric layer as the second electrode layer.

**[0006]** In this method of press-bonding the FPC onto the wiring lead-out via the anisotropic conductive member for coupling the wiring lead-out to the external wiring, the wiring lead-out is provided on the four sides which are the periphery of the PDP, and the electrodes are disposed in such a way that the potential applied to the wiring lead-out on each side is uniform. Accordingly, the wiring lead-out on each side is provided in the same plane to avoid coupling failure between the wiring lead-out and the FPC while press-bonding the FPC onto each side. If electrodes are given a multilayer structure by interposing the insulating layer, in addition to providing wiring lead-outs in such a way that the potential applied to each side is uniform, the electrode wiring in the second layer is disposed in such a way as to cross the step of insulating layer at the wiring lead-out. This makes the thickness of electrode wiring on the second layer thinner at this step, resulting in increasing the wiring resistance or causing disconnection.

**[0007]** The present invention aims to offer a highly reliable PDP by stabilizing the characteristics of the electrode wiring at the wiring lead-out even if the electrodes formed on the boards have a multilayer structure and their applied potential differs.

### DISCLOSURE OF INVENTION

**[0008]** A PDP of the present invention includes a front board having the first electrode that at least acts as a display electrode, and a rear board having the second electrode which at least acts as a data electrode and create a discharge space with the front board. The periphery of the front board and rear board is sealed to configure the PDP. The third electrode is disposed on the first electrode or second electrode with the dielectric layer in between. A lead-out of the first or second electrode to external wiring and a lead-out of the third electrode to external wiring are provided with a step equivalent to the thickness of the dielectric layer.

**[0009]** The above configuration allows the formation of each electrode in the same plane up to the wiring lead-out. This results in stable electrode wiring characteristics at the wiring lead-out, making feasible a highly reliable PDP.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]**

Fig. 1 is a sectional view of a PDP in accordance with the first exemplary embodiment of the present invention.

Fig. 2 is a perspective view of a rear board of the PDP in accordance with the first exemplary embodiment of the present invention.

Fig. 3 is a plan view of the rear board of the PDP in accordance with the first exemplary embodiment of the present invention.

Fig. 4 is a sectional view taken along A-A in Fig. 3.

Fig. 5 is a plan view of a sealed PDP in accordance with the first exemplary embodiment of the present invention.

Fig. 6 is a sectional view of a structure in which an FPC is connected to a wiring lead-out of the PDP in accordance with the first exemplary embodiment of the present invention.

Fig. 7A is a plan view illustrating a structure of the wiring lead-out of the PDP in accordance with the first exemplary embodiment of the present invention.

Fig. 7B is a sectional view taken along C-C in Fig. 7A.

Fig. 8A is a plan view illustrating a structure of a wiring lead-out of a PDP in accordance with the second exemplary embodiment of the present invention.

Fig. 8B is a sectional view taken along D-D in Fig. 8A.

Fig. 9A is a plan view of a structure illustrating a wiring lead-out of a PDP in accordance with the third exemplary embodiment.

Fig. 9B is a sectional view taken along E-E in Fig. 9A.

Fig. 10A is a plan view illustrating a structure of a wiring lead-out of a PDP in the fourth exemplary embodiment of the present invention.

Fig. 10B is a sectional view taken along F-F in Fig. 10A.

Fig. 11 is a sectional view of a PDP in the fifth exemplary embodiment of the present invention.

Fig. 128 is a sectional view taken along C-C in Fig. 12 A.

Fig. 13A is a plan view of a structure of the wiring lead-out when electrodes are disposed on a different level.

Fig. 13B is a sectional view taken along B-B in Fig. 13A.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENT(S)

**[0011]** Preferred embodiments of the present invention are described below with reference to drawings.

### FIRST EXEMPLARY EMBODIMENT

**[0012]** Fig. 1 shows a sectional view of a PDP in the first exemplary embodiment of the present invention. Fig. 2 is a perspective view of a rear board of the PDP in the first exemplary embodiment of the present invention.

**[0013]** As shown in Fig. 1, front board 1 and rear board 2 face each other with discharge space 3 in between. Gases such as neon (Ne) and xenon (Xe) are injected into this discharge space 3 and emit ultraviolet rays when subjected to electric discharge. The first electrode, which acts as a display electrode, includes stripes of a pair of scanning electrodes 6 and susutain electrodes 7 aligned in parallel and covered with dielectric layer 4 and protective film 5, and is disposed on front substrate 100. These scanning electrodes 6 and susutain electrodes 7 are configured, respectively, with transparent electrodes 6a and 7a, and metal bus lines 6b and 7b, made such as of silver (Ag) for better conductivity. Metal bus lines 6b and 7b are overlaid on transparent electrodes 6a and 7a. Moreover, scanning electrodes 6 and susutain electrodes 7 are alternately aligned in two rows each such as scanning electrode 6 - scanning electrode 6 - susutain electrode 7 - susutain electrode 7, and so on. Optical absorption film 8 made of black material is provided between rows of scanning electrodes 6 and between rows of susutain electrodes 7.

**[0014]** As shown in Figs. 1 and 2, stripes of data electrodes are disposed in parallel to each other on rear substrate 200 of rear board 2 as the second electrode in a direction perpendicular to scanning electrodes 6 and susutain electrodes 7. Moreover, barrier ribs 10 for dividing discharge cells formed with scanning electrodes 6, susutain electrodes 7, and data electrodes 9 are formed on rear board 2. Phosphor layer 12 corresponding to each discharge cell is formed on cell space 11 divided by barrier ribs 10. Barrier ribs 10 create cell space 11 with vertical wall 10a stretching so as to intersect at right angles with scanning electrodes 6 and susutain electrodes 7 on front board 1, i.e., parallel to data electrode 9; and horizontal wall 10b crossing this vertical wall 10a. Horizontal wall 10b also creates gap 13 between cell spaces 11. Optical absorption film 8 formed on front board 1 is disposed at positions corresponding to space in gap 13 formed between horizontal walls 10b of barrier rib 10.

**[0015]** In gap 13 of rear board 2, priming electrode 14, the third electrode, for triggering a discharge in the space of this gap 13 between front board 1 and rear board 2 is formed intersecting at right angles with data electrode 9. A priming cell is thus formed in gap 13. This priming electrode 14 is formed on dielectric layer 15 covering data electrode 9, and dielectric layer 16 is further formed to cover priming electrode 14. Accordingly, priming electrode 14 is formed in a position closer to the space of gap 13 than data electrode 9. In addition, priming electrode 14 is formed only at the position of gap 13 opposing adjacent scanning electrodes 6 to which a scanning pulse is applied. A part of metal bus

line 6b of scanning electrode 6 extends to the position corresponding to gap 13, and is formed on optical absorption film 8. In other words, priming discharge occurs between metal bus line 6b protruding toward area of gap 13 and priming electrode 14 formed on rear board 2.

**[0016]** In the PDP, front board 1 and rear board 2 face each other such that data electrode 9 and scanning electrode 6, and susutain electrode 7 intersect at right angles; and their peripheries are hermetically sealed. In cell space 11 formed by barrier rib 10, discharge spaces 17R, 17G and 17B for red, green and blue are created, and phosphor layer 12 of each color is formed on the wall of each discharge space. Discharge gases such as neon (Ne) - Xenon (Xe) are injected under a pressure of 400 ~ 600 torr. Discharge gas is discharged by selectively applying the video signal voltage to the scanning electrodes 6 and susutain electrodes 7. As a result, the ultraviolet rays emitted excite phosphor layer 12 of each color, and a color image is displayed when the phosphor emits red, green and blue colors. Moreover, in the PDP in this exemplary embodiment, priming discharge takes place in gap 13 so as to reduce discharge delay in writing. This realizes a PDP achieving a stable address characteristic, such as in a high-definition panel.

**[0017]** Fig. 3 shows a plan view of rear board 2 of the PDP in the first exemplary embodiment of the present invention, and Fig. 4 shows a sectional view taken along A-A in Fig. 3. Priming electrode 14, the third electrode, indicated by the broken line in Fig. 3, is formed only at gap 13, corresponding to adjacent scanning electrodes 6 to which a scanning pulse is applied, and the same potential is applied within the face of the PDP. This potential is different from that given to scanning electrodes 6 and susutain electrodes 7 configuring the first electrode and data electrodes 9 configuring the second electrode. Moreover, wiring lead-out 18 of priming electrode 14 is provided at the four corners of rear board 2, and dielectric layer 16 covers priming electrode 14 except for these wiring lead-outs 18. Dielectric layer 15 covers data electrodes 9 except for their wiring lead-outs 19. Accordingly, as shown in Fig. 4, wiring lead-outs 18 and wiring lead-outs 19 have step 20, equivalent to the film thickness of dielectric layer 15.

**[0018]** On the other hand, scanning electrodes 6, susutain electrodes 7, and data electrodes 9 of the PDP are connected to an electric circuit for driving and controlling electrodes using an FPC. Fig. 5 shows a plan view of a PDP in which front board 1 and rear board 2 are sealed, seen from the side of front board 1. Wiring lead-outs 19 of data electrodes 9 are provided at upper edge 22 and lower edge 21 of rear board 2 in several blocks.

**[0019]** Fig. 6 shows a sectional view of a part where FP C 23 for connecting to external wiring is attached to wiring lead-out 19 of data electrode 9 when lead-out electrodes are in the same plane. FPC 23 has multiple wiring patterns 25, made such as of copper foil, formed on resin base film 24 that acts as a flexible insulator such as polyimide. A connecting portion at the end of wiring pattern 25 is exposed and the other portion of wiring pattern 25 is covered with resin cover film 26 such as polyimide. Wiring pattern 25 is connected to data electrode 9 of wiring lead-out 19 via anisotropic conductive material 27, and its periphery is covered with adhesive 28. Anisotropic conductive material 27 is made by dispersing conductive particles such as nickel (Ni) in an insulating material. Although anisotropic conductive material 27 shows no conductivity as it is, connection is established when conductive particles bond in the space between data electrode 9 and wiring patterns 25 as a result of sandwiching conductive particles between rear board 2 and FPC 23, and intensely compressing the insulating material by means of thermal pressing.

**[0020]** Fig. 13A is a plan view illustrating a wiring lead-out structure for leading out the electrode when a step exists between the electrodes in the PDP. Fig. 13B is a sectional view taken along B-B in Fig. 13A. One of the four corners shown in the plan view of rear board 2 in Fig. 3 is magnified. As shown in Figs. 13A and 13B, data electrode 9 and priming electrode 14 are provided in the same plane at the wiring lead-outs so as to simplify process including press-bonding of the FPC. More specifically, dielectric layer 15 is provided on rear substrate 200 and priming electrode 14 is disposed on dielectric layer 15, but wiring of priming electrode 14 and wiring of data electrode 9 are led out in the same plane of rear substrate 200 at the edge of rear substrate 200.

**[0021]** In this case, priming electrode 14 has step 40 equivalent to the thickness of dielectric layer 15. If the electrode wiring is stepped, the wiring thickness differs at the step, increasing wiring resistance at the thinned portion. This results in an inability to drive signals at high speed due to significant delay in carrying the signals. Accordingly, this step becomes a major obstacle to increasing pixel density to achieve higher-definition PDPs. In addition, such step likely to cause disconnection of electrodes, significantly reducing reliability.

**[0022]** Figs. 7A and 7B show the detailed structure of the wiring lead-out of the PDP shown in Figs. 3 and 4 in the first exemplary embodiment. Fig. 7A is a plan view, and Fig. 7B is a sectional view taken along C-C in Fig. 7A. In the first exemplary embodiment, wiring lead-out 18 of priming electrode 14 is formed on dielectric layer 15. In other words, the level of wiring lead-out 19 of data electrode 9 and wiring lead-out 18 of priming electrode 14 is different for step 20 equivalent to the thickness of dielectric layer 15, as shown in Fig. 4. Accordingly, data electrode 9 is connected to the FPC and priming electrode 14 is connected to the FPC at a different level, equivalent to step 20.

**[0023]** Priming electrode 14, the third electrode in the present invention, is an electrode that gives the same potential in the PDP face. This potential is different from that of other electrodes. This means that the function of priming electrode 14 is achievable with at least one wiring lead-out 18, although wiring lead-out 18 is provided at the four corners in Fig. 3. The FPC connection to wiring lead-out 19 of data electrode 9 can thus be established in a separate process. Accordingly, priming electrode 14 can be formed in the same plane, eliminating stepped electrode wiring and allowing

signals to be driven at high speed. In addition, failures such as disconnection due to variable wiring thickness of electrodes and degradation by heat generated due to high wiring resistance can be reduced, making feasible a PDP with highly reliable wiring.

**[0024]** In the first exemplary embodiment, the wiring lead-out direction of priming electrode 14 and the wiring lead-out direction of data electrode 9 are the same, but are not necessarily leading in the same direction, depending on the pattern of dielectric layer 15.

SECOND EXEMPLARY EMBODIMENT

**[0025]** Figs. 8A and 8B show details of a structure of a wiring lead-out of a PDP in the second exemplary embodiment of the present invention. Fig. 8A is a plan view, and Fig. 8B is a sectional view taken along D-D in Fig. 8A.

**[0026]** In the second exemplary embodiment, slope 31 is provided in the wiring lead-out area of priming electrode 14. In this slope 31, the film thickness of dielectric layer 15 gradually reduces in a slope toward the edge of rear substrate 200, and wiring lead-out 29 is formed on rear substrate 200. Accordingly, priming electrode 14 and data electrode 9 are in the same plane at wiring lead-out 29 connected to the FPC.

**[0027]** As described above, the thickness of dielectric layer 15 is gradually reduced in the wiring lead-out area of priming electrode 14 such that there is no effect of reduced thickness or line width of priming electrode 14 that is formed on dielectric layer 15. This secures the reliability of wiring of priming electrode 14. Moreover, connection to the FPC is established in the same plane as wiring lead-out 19 of data electrode 9. This allows connection of priming electrode 14 to the FPC and connection of data electrode 9 to the FPC in the same process, simplifying the manufacturing process. Furthermore, provision of priming electrode 14 and data electrode 9 in the same plane allows sharing of the wiring FPC between priming electrode 14 and data electrode 9.

**[0028]** The thickness of dielectric layer 15 can be reduced step by step or linearly as long as the thickness is changed in a way such that to eliminate any non-uniformity in electrode thickness and line width when forming priming electrode 14 on dielectric layer 15.

THIRD EXEMPLARY EMBODIMENT

**[0029]** Figs. 9A and 9B show the details of a structure of wiring lead-out of a PDP in the third exemplary embodiment. Fig. 9A is a plan view, and Fig. 9B is a sectional view taken along E-E in Fig. 9A.

**[0030]** In the third exemplary embodiment, priming electrode wiring 33 formed on rear substrate 200 in advance and priming electrode 14 formed on dielectric layer 15 are connected by via hole 32 created on dielectric layer 15. This via hole is filled with conductive material. Accordingly, wiring lead-out 30 to be connected to the FPC is formed in the same plane as data electrode 9.

**[0031]** Via hole 32 is created such as by laser beam after forming dielectric layer 15, and the conductive material is injected into via hole 32. This method secures the wiring reliability of priming electrode 14. In addition, connection to the FPC is established in the same plane as wiring lead-out 19 of data electrode 9. This allows wiring to be carried out in the same process as connection of the FPC to data electrode 9, simplifying the manufacturing process.

FOURTH EXEMPLARY EMBODIMENT

**[0032]** Figs. 10A and 10B show details of the structure of a wiring lead-out in the fourth exemplary embodiment of the present invention. Fig. 10A is a plan view illustrating the structure of a rear board, and Fig. 10B is a sectional view taken along F-F in Fig. 10A.

**[0033]** As shown in Figs. 10A and 10B, priming electrode 14 includes vertical priming electrode 34 and horizontal priming electrode 35. Vertical priming electrode 34 also acts as wiring lead-out of priming electrode 14. Vertical priming electrode 34 is formed on rear substrate 200, same as data electrode 9, and horizontal priming electrode 35 is formed on dielectric layer 15. A dielectric layer can be further formed on horizontal priming electrode 35. Via hole 36 is created on dielectric layer 15 at crossing of vertical priming electrode 34 and horizontal priming electrode 35. Conductive material is injected into via hole 36 to secure mutual conductivity.

**[0034]** The above structure enables formation of vertical priming electrode 34 at the same time as forming data electrode 9 on rear substrate 200. In addition, wiring lead-out 18 of priming electrode 14 can be connected to the FPC in the same plane as wiring lead-out 19 of data electrode 9. Accordingly, this connection can be established in the same process as connection of data electrode 9 to the FPC, thus simplifying the process.

FIFTH EXEMPLARY EMBODIMENT

**[0035]** Fig. 11 is a sectional view of a PDP in the fifth exemplary embodiment of the present invention. As shown in

Fig. 11, the structures of data electrode 9, i.e., the second electrode, and priming electrode 14, i.e., the third electrode, formed on rear substrate 200 differ from those in the first exemplary embodiment.

**[0036]** More specifically, in the fifth exemplary embodiment, priming electrode 14 is first formed on rear substrate 200. Dielectric layer 15 is then provided covering priming electrode 14. Data electrode 9 is then disposed on dielectric layer 15. Moreover, dielectric layer 16 that also acts as a base for forming barrier ribs is provided covering data electrode 9. Barrier rib 10 is formed on this dielectric layer 16. As described above, the fifth exemplary embodiment has a different structure for rear substrate 200, but the same structure as the first exemplary embodiment for front substrate 100.

**[0037]** Accordingly, the fifth exemplary embodiment has data electrode 9 formed closer to discharge space 3 than priming electrode 14. This allows a thinner dielectric layer 16 to be formed on data electrode 9, enabling lower voltage during write discharge. Write discharge can thus be stabilized. Dielectric layer 15, formed on priming electrode 14, is a dielectric layer between priming electrode 14 and data electrode 9, and any material at any thickness can be applied to secure insulation between priming electrode 14 and data electrode 9.

**[0038]** The structure described in the first to fourth exemplary embodiments is applicable to the structure of wiring lead-out 18 of priming electrode 14 and wiring lead-out 19 of data electrode 9 in the fifth exemplary embodiment. However, the positions of priming electrode 14 and data electrode 9 in the fifth embodiment are upside down with respect to dielectric layer 15.

**[0039]** As an example, the structure of the wiring lead-out identical to that described in the first exemplary embodiment is shown in Figs. 12A and 12B. In the structure of the first exemplary embodiment shown in Figs. 7A and 7B, wiring lead-out 18 of priming electrode 14 is provided on dielectric layer 15. However, in the fifth exemplary embodiment, wiring lead-out 50 of data electrode 9 is provided on dielectric layer 15, and wiring lead-out 51 of priming electrode 14 is provided on rear substrate 200. Accordingly, a PDP with highly reliable wiring can be realized by securing stable wiring even though the positions of data electrode 9 and priming electrode 14 are reversed.

**[0040]** In the above exemplary embodiments, dielectric layer 15 or dielectric layer 16 has a patterned shape at the wiring lead-out. This pattern can be formed using known methods including screen-printing and photo etching.

**[0041]** Furthermore, the above exemplary embodiments refer to the case of the two-layer electrode on the rear board. It is apparent, however, the structure of the present invention is not limited to the rear board. Naturally, the wiring lead-out structure of the present invention is also applicable to a multilayer structure of two or more layers for the front board or for both front and rear boards.

## INDUSTRIAL APPLICABILITY

**[0042]** The present invention employs a structure without a step in the electrode wiring at the wiring lead-out of the PDP. This eliminates variations in the wiring thickness of the electrode, and problems deriving from the resultant high wiring resistance. Accordingly, a highly reliable PDP suitable for a large-screen display device is achieved.

Reference marks in the drawings

**[0043]**

| | |
|---|---|
| 1 | Front board |
| 2 | Rear board |
| 3 | Discharge space |
| 4, 15, 16 | Dielectric layer |
| 5 | Protective film |
| 6 | Scanning electrode |
| 6a, 7a | Transparent electrode |
| 6b, 7 b | Metal bus line |
| 7 | Susutain electrode |
| 8 | Optical absorption film |
| 9 | Data electrode |
| 10 | Barrier rib |
| 10a | Vertical wall |
| 1 0b | Horizontal wall |
| 11 | Cell space |
| 1 2 | Phosphor layer |
| 13 | Gap |
| 1 4 | Priming electrode |
| 17, 17B, 17G, 17R | Discharge space |

| | |
|---|---|
| 18, 19, 29, 30, 50, 51 | Wiring lead-out |
| 20, 40 | Step |
| 21 | Lower edge |
| 22 | Upper edge |
| 23 | FPC |
| 24 | Base film |
| 25 | Wiring pattern |
| 26 | Cover film |
| 27 | Anisotropic conductive material |
| 28 | Adhesive |
| 31 | Slope |
| 32, 36 | Via hole |
| 33 | Priming electrode wiring |
| 34 | Vertical priming electrode |
| 35 | Horizontal priming electrode |
| 100 | Front substrate |
| 200 | Rear substrate |

## Claims

1. A plasma display panel comprising:

   a front board having a first electrode which at least acts as a display electrode; and
   a rear board having a second electrode which at least acts as a data electrode, the rear board forming a discharge space with the front board; and peripheries of the front board and rear board being sealed;

   wherein a third electrode is provided on at least one of the first electrode and the second electrode with a dielectric layer in between, and an external wiring lead-out of one of the first electrode and the second electrode and an external wiring lead-out of the third electrode are provided with a step equivalent to a thickness of the dielectric layer.

2. A plasma display panel comprising:

   a front board having a first electrode which at least acts as a display electrode; and
   a rear board having a second electrode which at least acts as a data electrode, the rear board forming a discharge space with the front board; and peripheries of the front board and rear board being sealed;

   wherein a third electrode is provided on at least one of the first electrode and the second electrode with a dielectric layer in between, and an external wiring lead-out of one of the first electrode and the second electrode and an external wiring lead-out of the third electrode are provided in the same plane.

3. The plasma display panel as defined in Claim 2, wherein a thickness of the dielectric layer is reduced inclining toward at least one of the wiring lead-out of one of the first electrode and second electrode and the wiring lead-out of the third electrode.

4. The plasma display panel as defined in Claim 2, wherein at least one of the wiring lead-out of one of the first electrode and second electrode and the wiring lead-out of the third electrode is provided on a lead-out electrode provided in the same plane as an other wiring lead-out through a via hole formed on the dielectric layer.

5. The plasma display panel as defined in one of Claims 1 and 2, wherein the third electrode gives the same potential within a face of the plasma display panel.

6. The plasma display panel as defined in Claim 5, wherein a potential applied to the third electrode is at least different from a potential applied to the first electrode and the second electrode.

7. The plasma display panel as defined one of Claims 1 and 2, wherein the third electrode is a priming electrode.

FIG.1

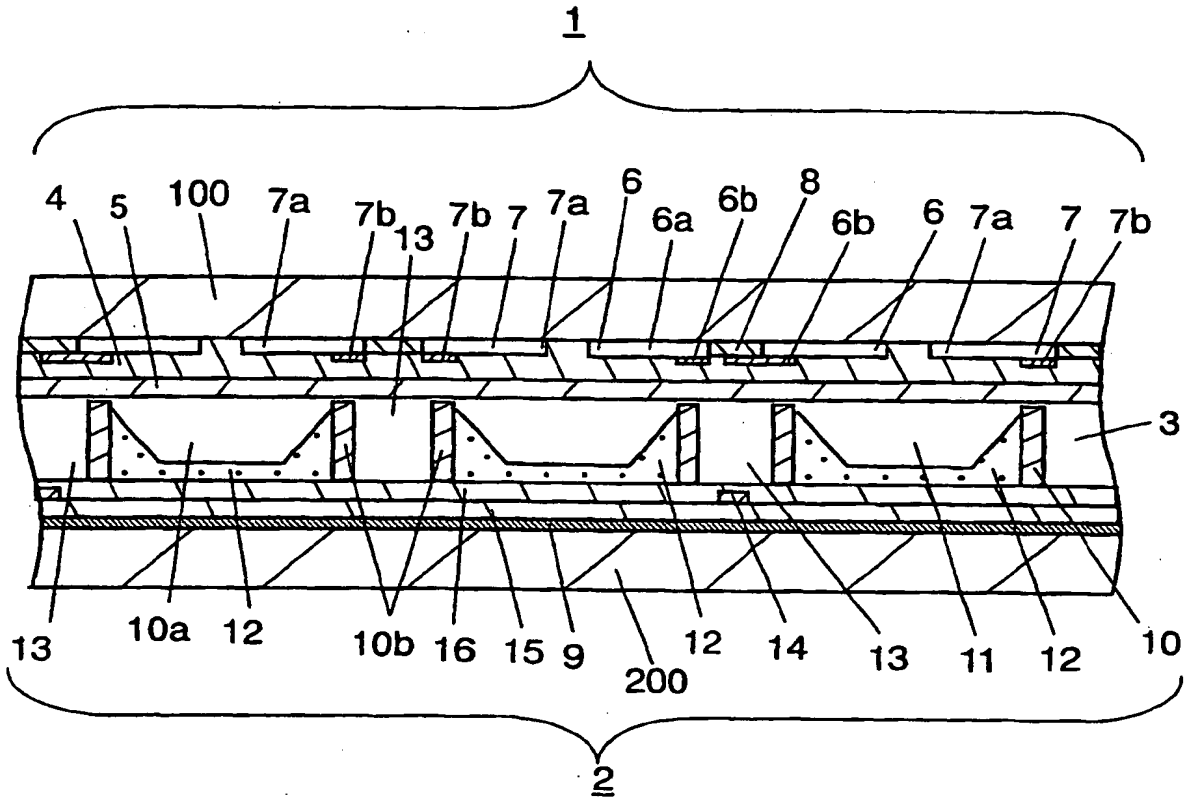


FIG.2

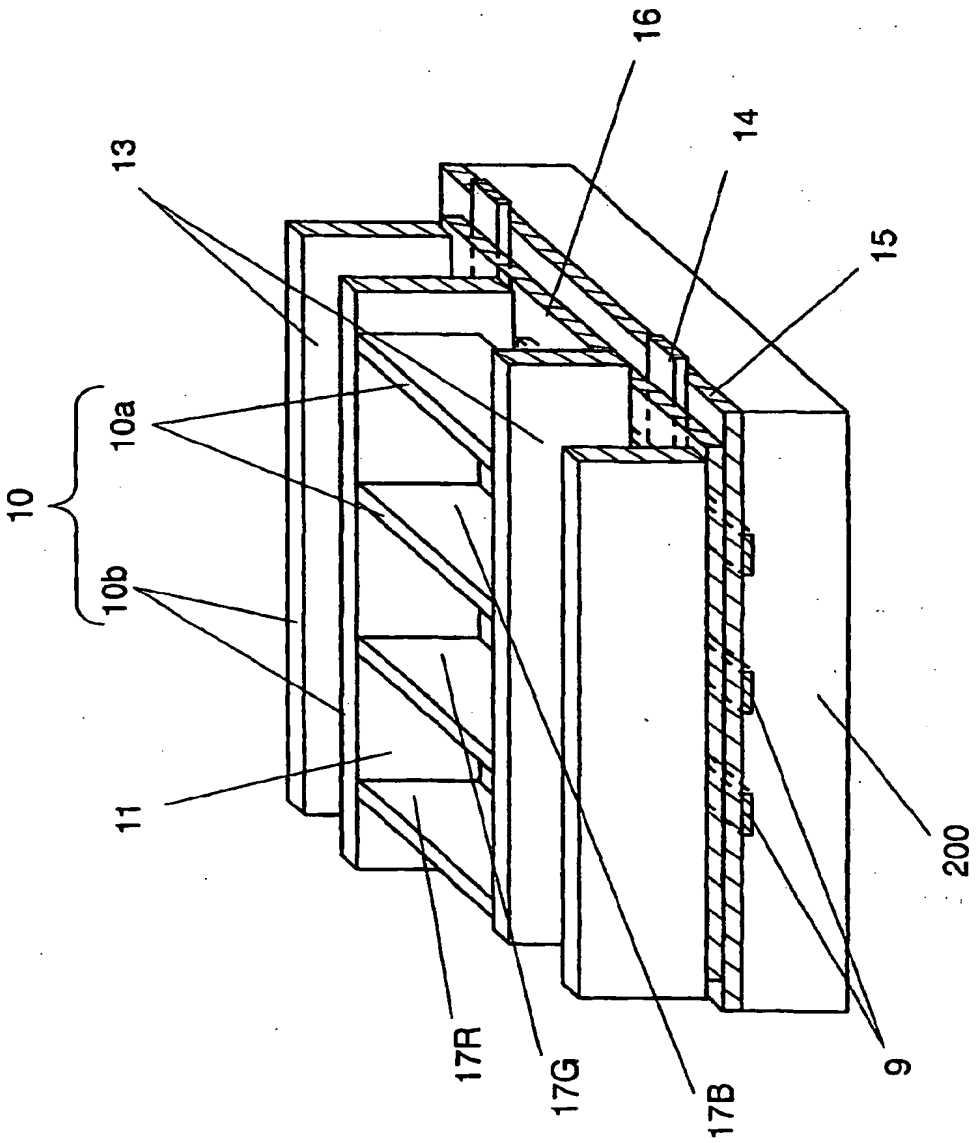


FIG.3

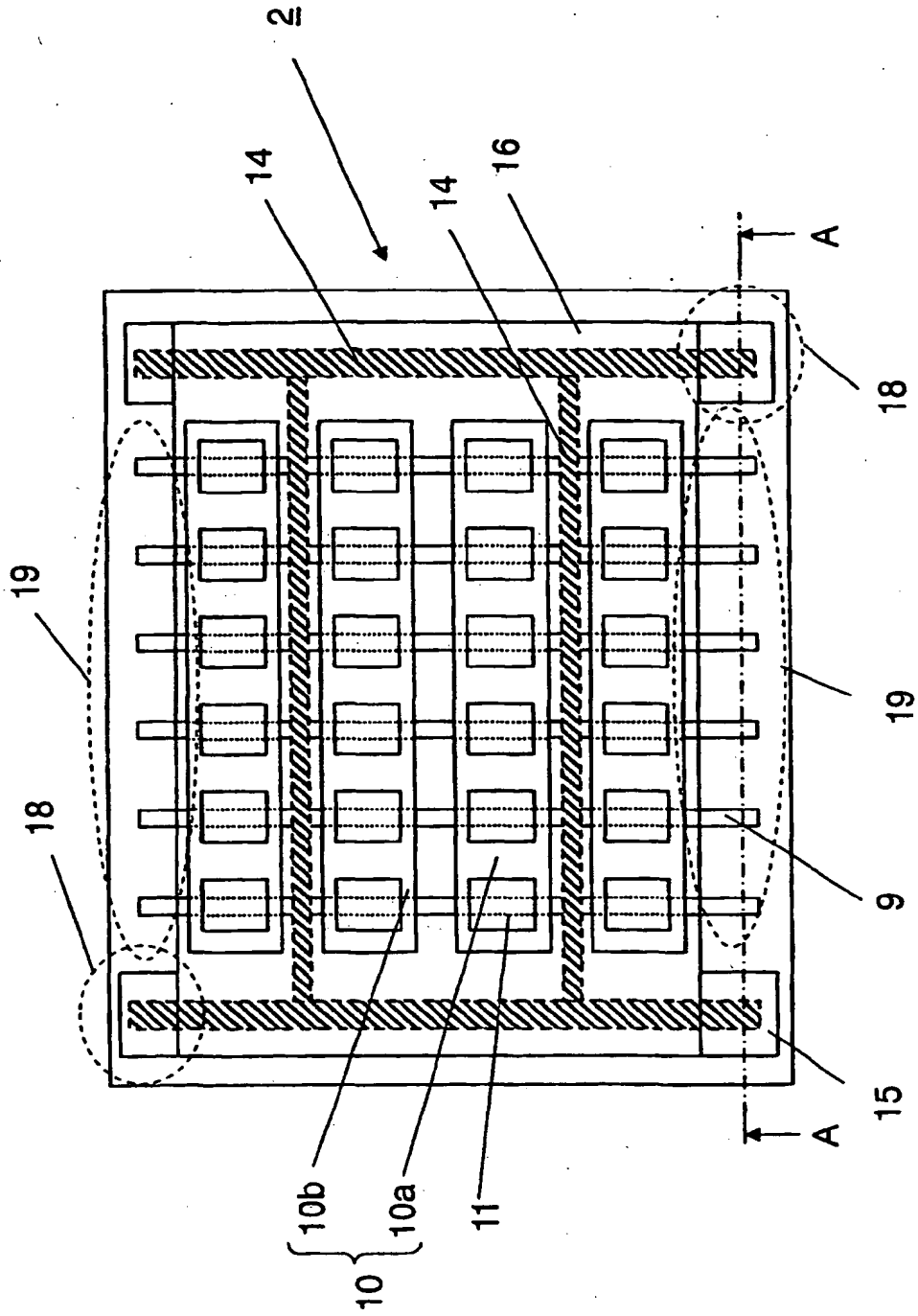


FIG.4

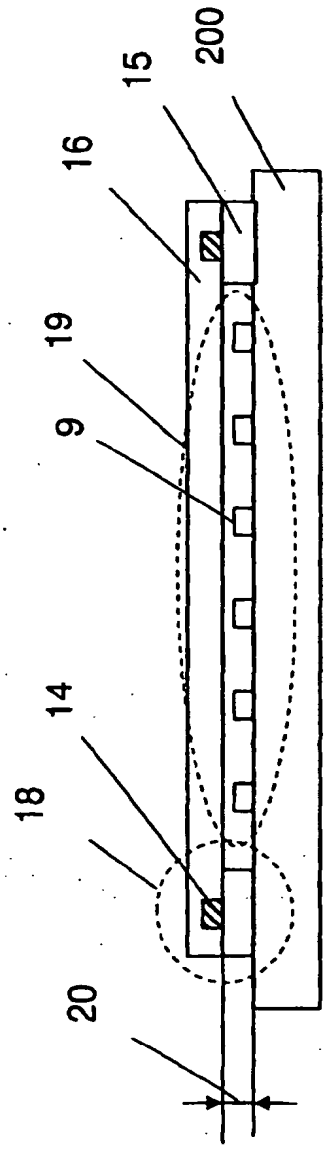


FIG.5

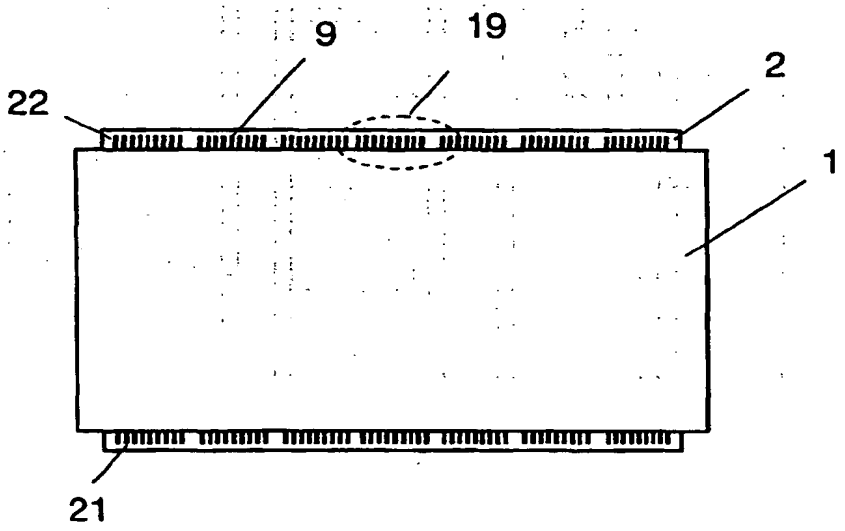


FIG.6

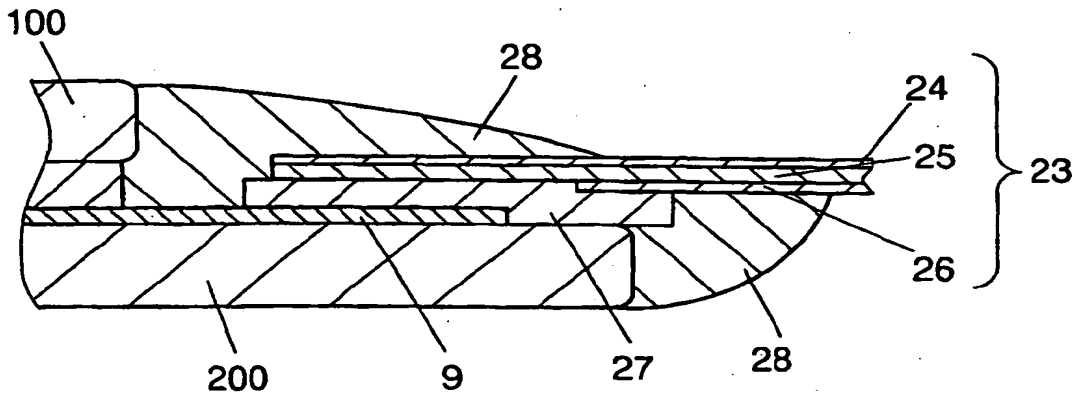


FIG.7B

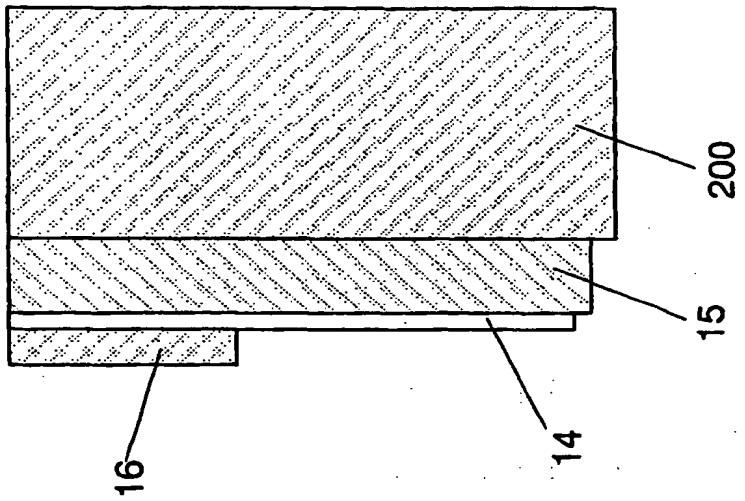



FIG.7A

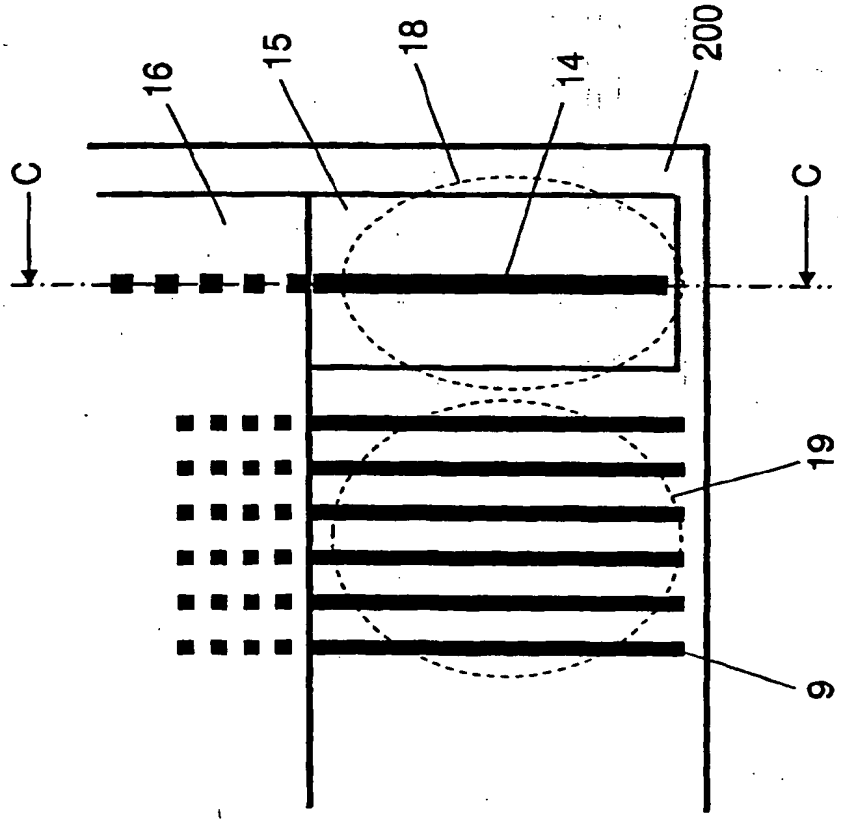


FIG.8B

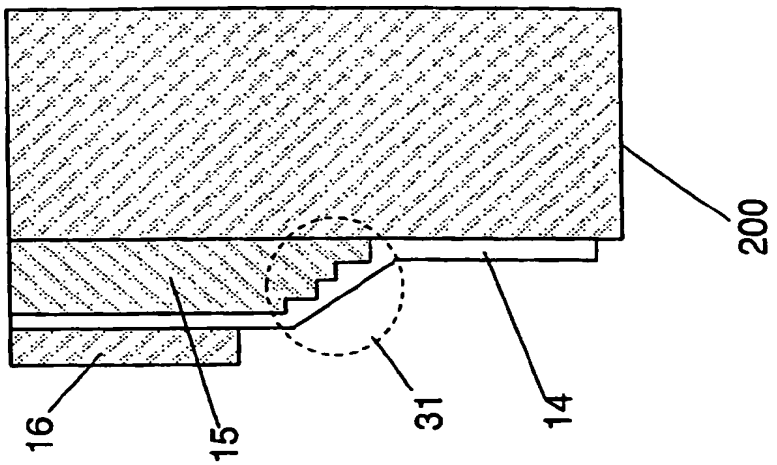



FIG.8A

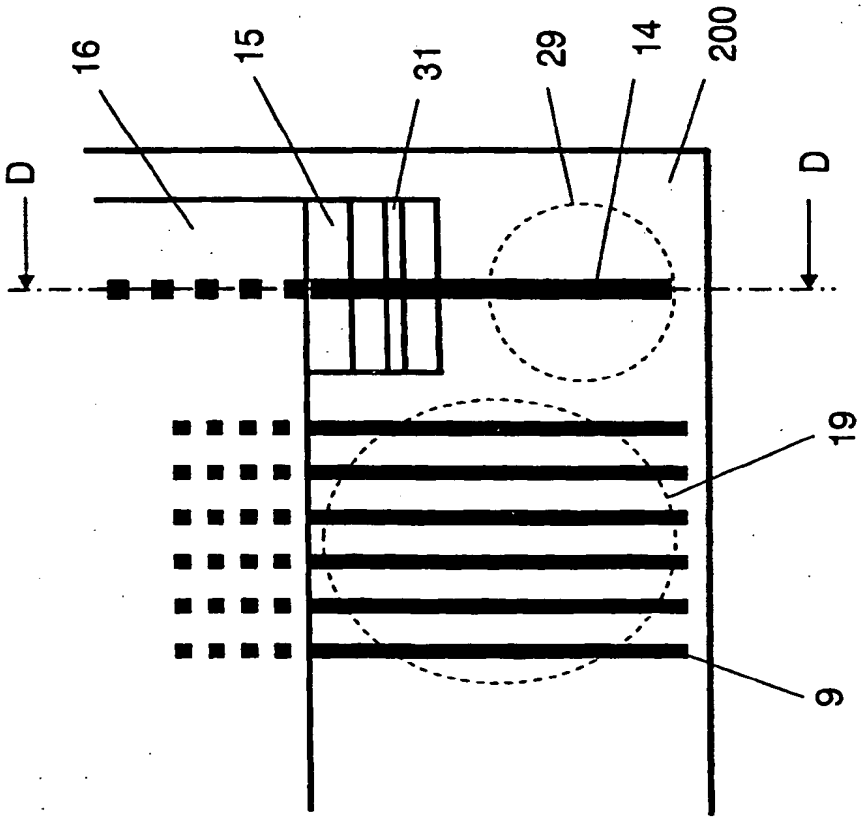


FIG.9B

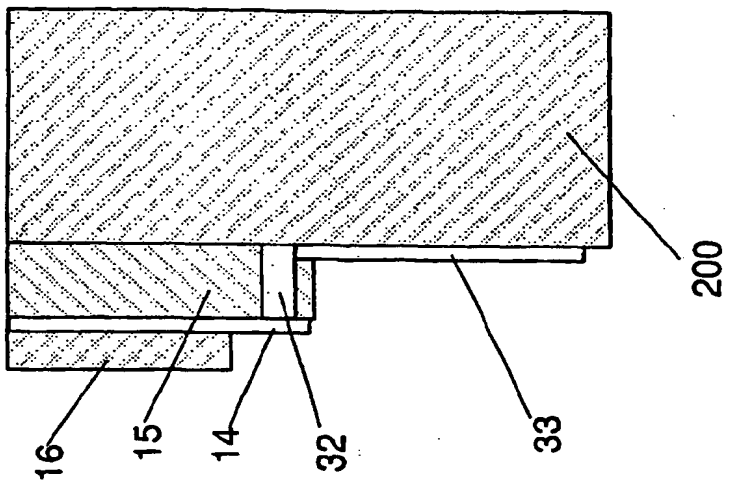



FIG.9A

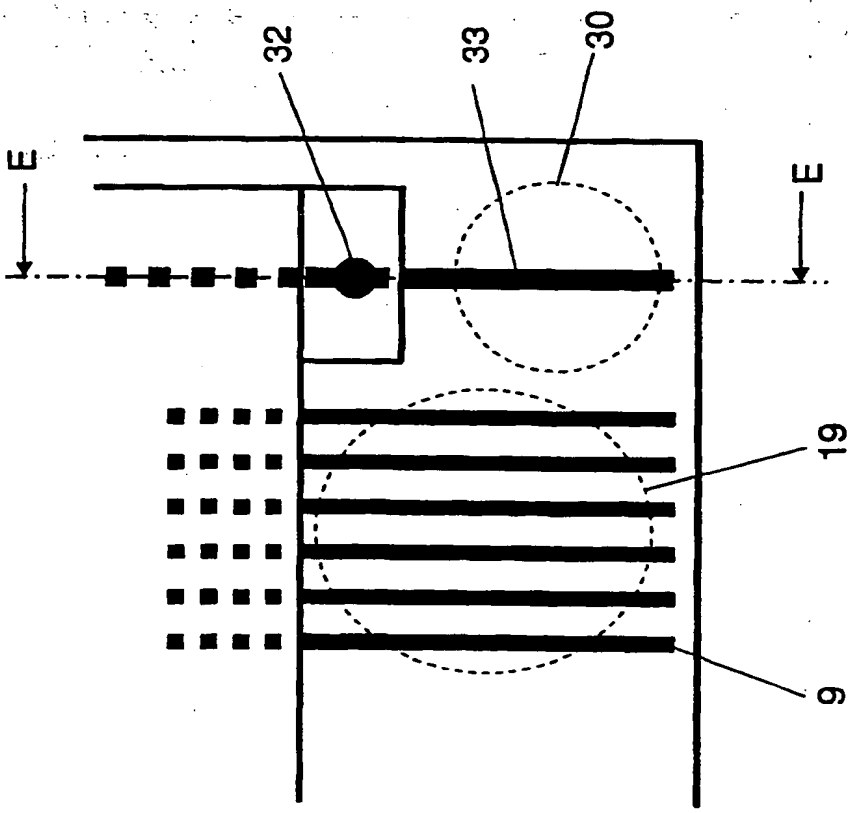


FIG.10B

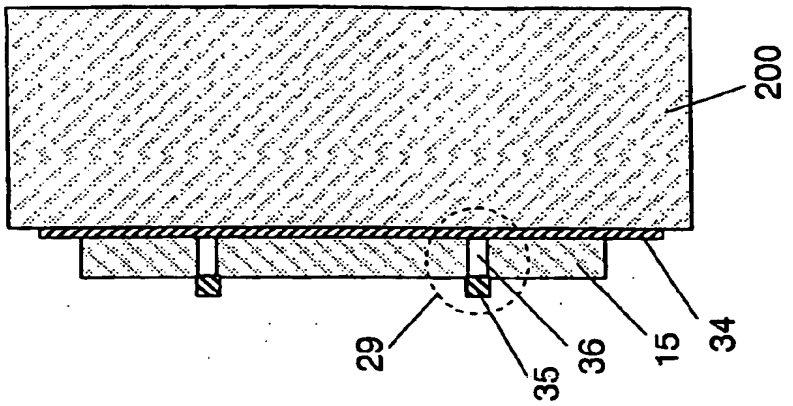



FIG.10A

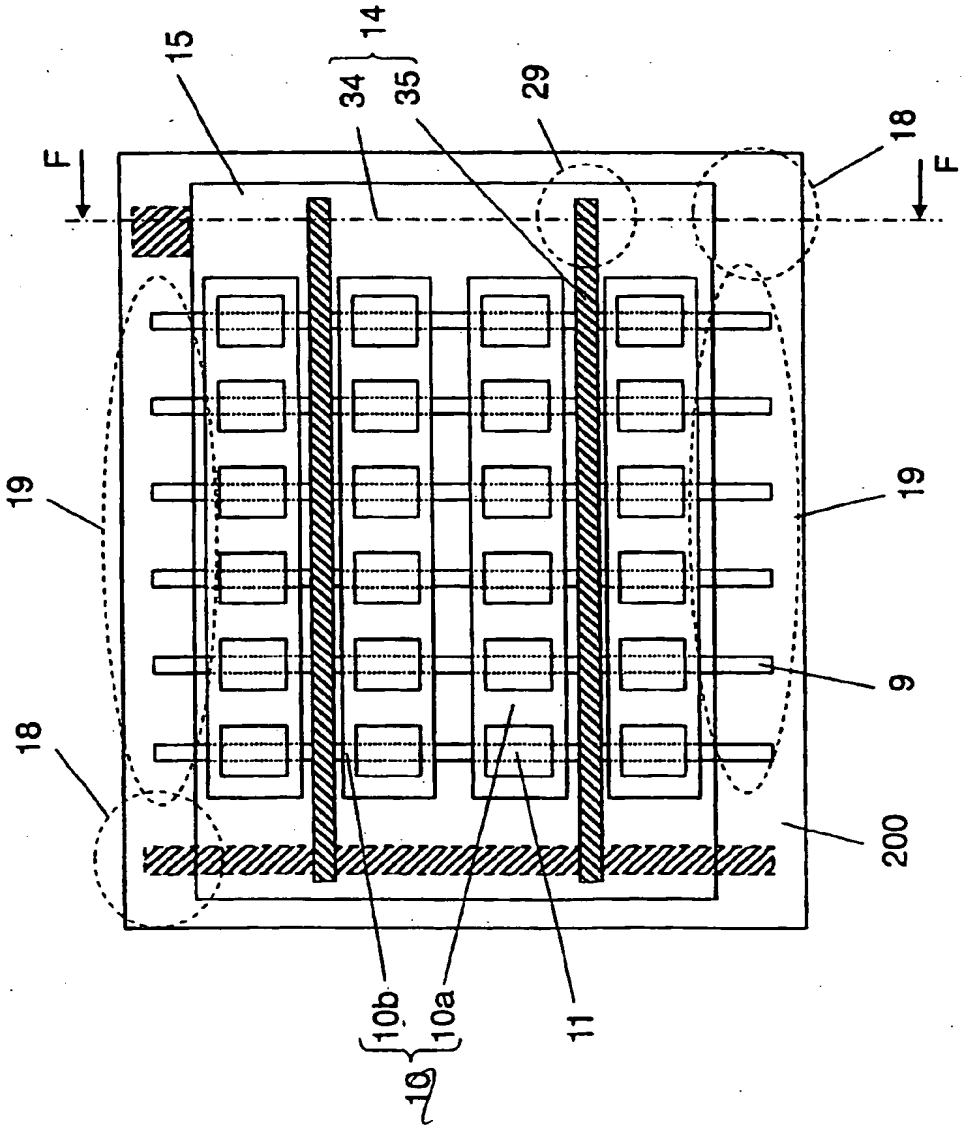


FIG.11

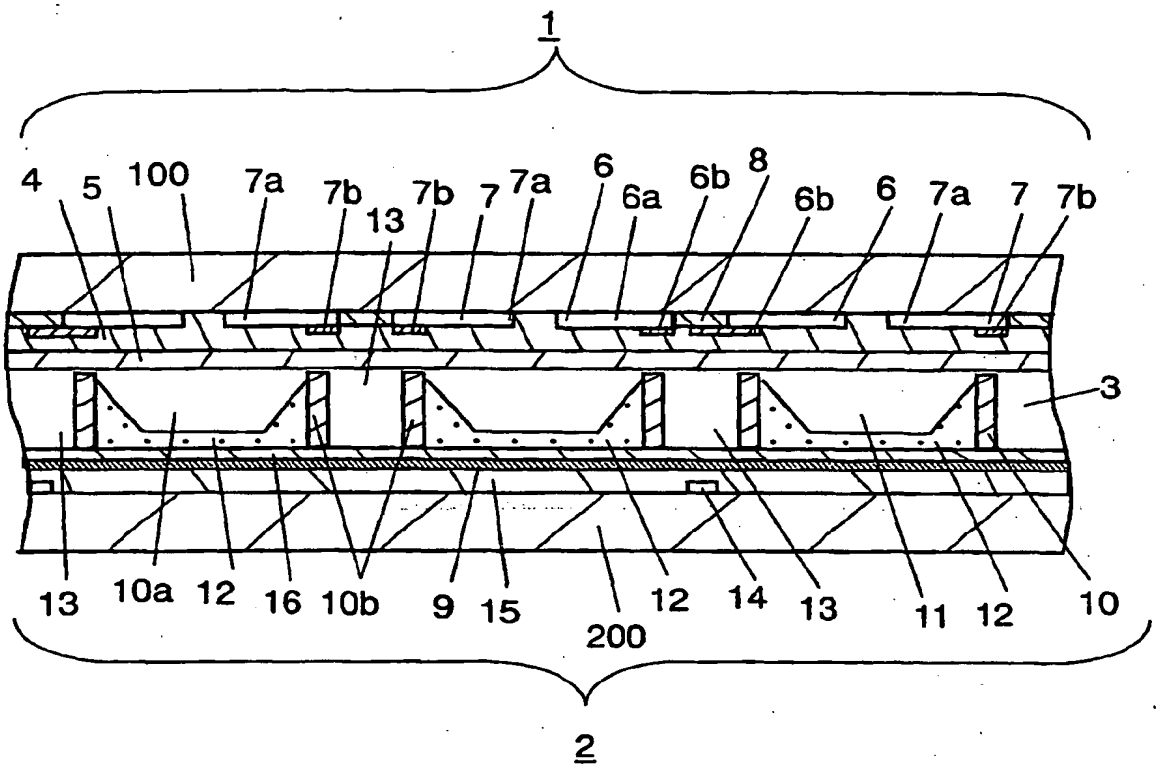


FIG.12B

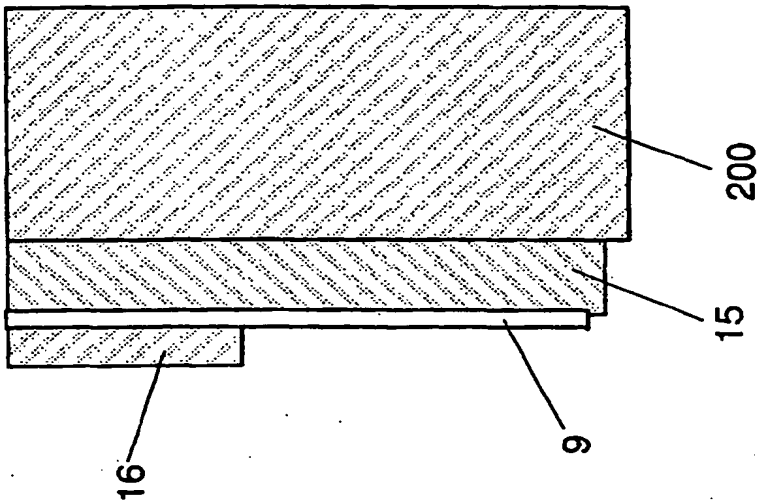



FIG.12A

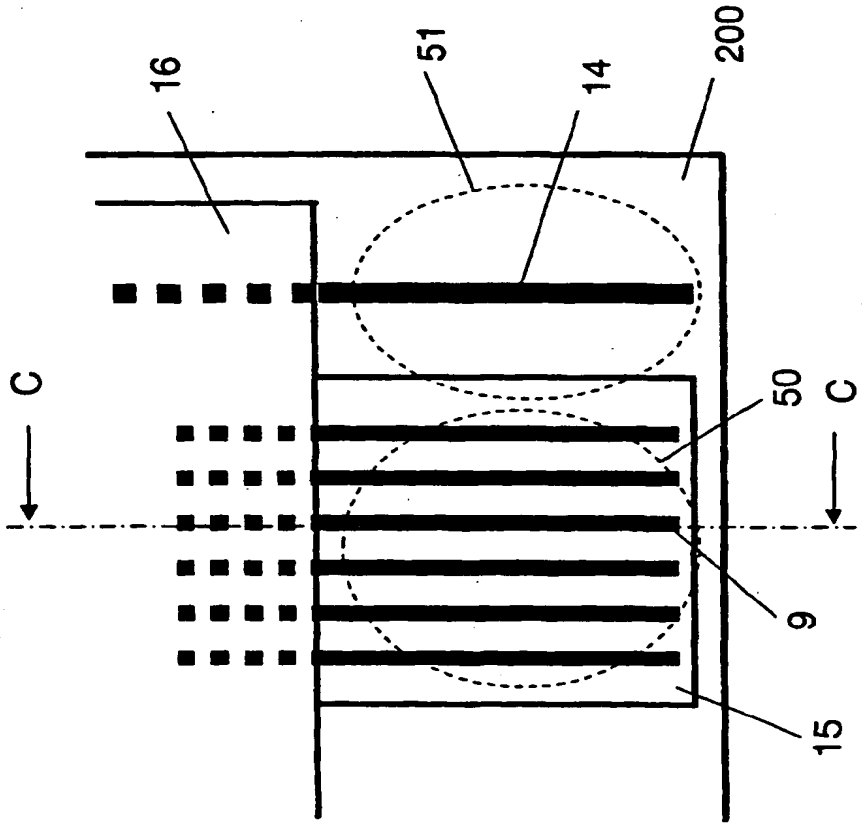


FIG.13B

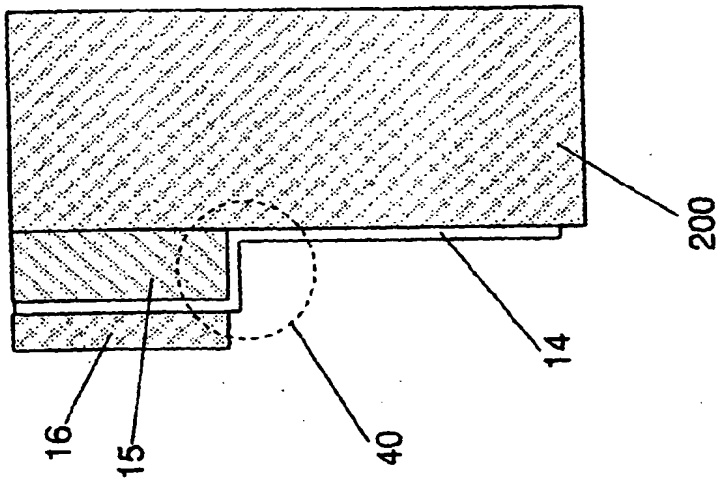
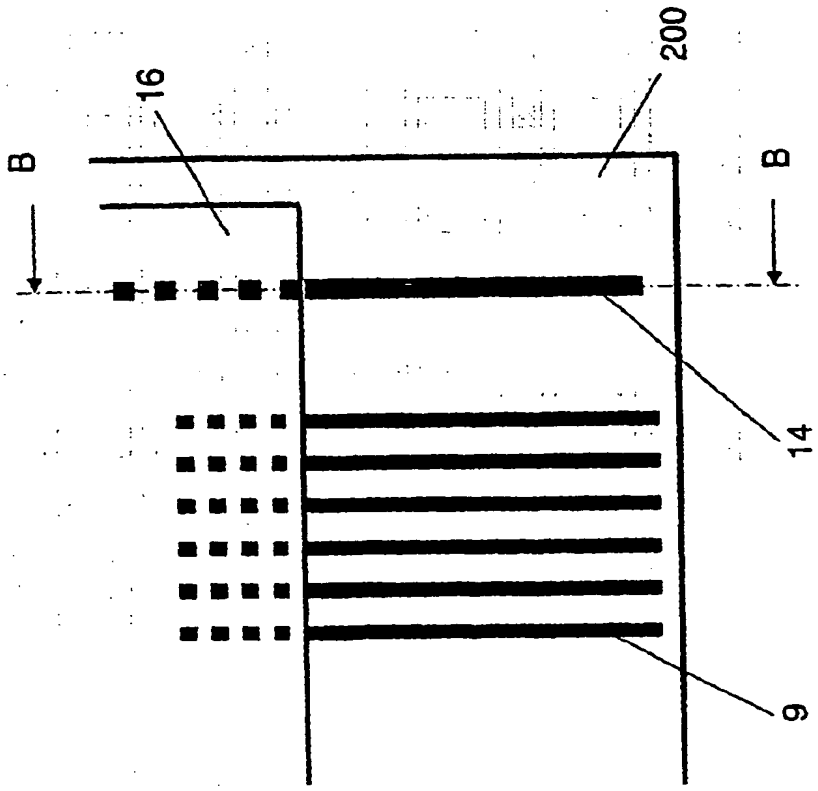



FIG.13A



## INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/001811

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01J11/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01J11/00-04, 17/00-49, 9/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2004
Kokai Jitsuyo Shinan Koho 1971-2004 Jitsuyo Shinan Toroku Koho 1996-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>Y | JP 9-259768 A (Fujitsu Ltd.),<br>03 October, 1997 (03.10.97),<br>Par. Nos. [0017] to [0024]; Figs. 1 to 3<br>(Family: none) | 1,2<br>3-7 |
| Y | JP 2002-50300 A (Karl Zmyis Schifuzing),<br>15 February, 2002 (15.02.02),<br>Par. No. [0012]; Fig. 1<br>& EP 1164623 A2 & US 2002/0024498 A1 | 3 |
| Y | JP 6-236734 A (Nippon Hoso Kyokai),<br>23 August, 1994 (23.08.94),<br>Par. Nos. [0021], [0022]; Fig. 8<br>(Family: none) | 4 |

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 18 May, 2004 (18.05.04) | 08 June, 2004 (08.06.04) |
| Name and mailing address of the ISA/<br>Japanese Patent Office | Authorized officer |
| Facsimile No. | Telephone No. |

Form PCT/ISA/210 (second sheet) (January 2004)

**INTERNATIONAL SEARCH REPORT**

International application No.
PCT/JP2004/001811

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | JP 5-2992 A (Matsushita Electronics Corp.), 08 January, 1993 (08.01.93), Par. No. [0008]; Fig. 1 (Family: none) | 5-7 |
| A | JP 5-250994 A (Mitsubishi Electric Corp.), 28 September, 1993 (28.09.93), Par. Nos. [0009] to [0012]; Figs. 3, 4 & US 5405494 A & US 5428263 A | 1-7 |
| A | JP 8-96714 A (NEC Corp.), 12 April, 1996 (12.04.96), Full text; all drawings (Family: none) | 1-7 |

Form PCT/ISA/210 (continuation of second sheet) (January 2004)